CLAIMS

1. Voltage regulator with an output transistor (MP1), comprising:

a first PMOS FET, whereby the input voltage (Vdd) of the voltage regulator is applied to the source of the output transistor (MP1) and where the drain of the output transistor (MP1) serves as the output of the voltage regulator,

a regulation circuit (1) that is configured so as to output an error signal representing the deviation of the actual output voltage (Vout) of the voltage regulator from the target output voltage of the voltage regulator at its output, the output of the regulating circuit (1) being connected to the gate of the output transistor (MP1), which is controlled by the error signal in such a way that any deviations between the output voltage (Vout) and the target output voltage are minimized, as well as a switch-on protection circuit,

a second PMOS FET (MP2), the source of the second PMOS FET (MP2) being connected to the input voltage (Vdd) of the voltage regulator, the drain of the second PMOS FET (MP2) by way of a pulldown resistor R3) to a reference potential (Vss), and the gate of the second PMOS FET (MP2) to the reference potential (Vss), and

a third PMOS FET (MP3), where the source of the third PMOS FET (MP3) is connected to the input voltage (Vdd) of the voltage regulator, the drain of the third PMOS FET (MP3) is connected to the gate of the output transistor (MP1), and the gate of the third PMOS FET (MP3) is connected to the drain of the second PMOS FET (MP2).

2. Voltage regulator according to Claim 1, wherein the regulation circuit is compares a reference voltage (Vref), which defines the target output voltage of the voltage regulator, with a voltage that represents the actual output voltage (Vout) of the voltage regulator.

3. Voltage regulator according to Claim 2, wherein the regulation circuit (1) is an operational amplifier.

4. Voltage regulator according to Claim 1, wherein the reference potential (Vss) is the ground potential.

5. Voltage regulator according to Claim 1, wherein the voltage representing the actual output voltage (Vout) is derived from the output voltage (Vout) by way of a voltage divider (R1, R2).

6. Voltage regulator according to Claim 1, where the switch-on protection circuit furthermore comprises an RC combination that is connected to the source-drain path of the second PMOS FET (MP2).

7. Voltage regulator according to Claim 6, where the capacitor (C) of the RC combination is connected between the drain of the second PMOS FET (MP2) and the reference potential Vss), and the resistor (R4) of the RC combination is connected between the input voltage Vdd) of the voltage regulator and the source of the second PMOS FET (MP2).

8. Voltage regulator according to Claim 1, where the switch-on protection circuit furthermore comprises an NMOS FET (MN1) that is connected so as to force the output voltage (Vout) of the voltage regulator to assume the reference potential (Vss) whilst the voltage regulator is switched on.

9. Voltage regulator according to Claim 8, where the source of the NMOS FET (MN1) is connected to the reference potential (Vss), the drain of the NMOS FET (MN1) to the output of the voltage regulator, and the gate of the NMOS FET (MN1) is connected to the reference potential by way of a further pull-down resistor (R5), whereby the switch-on protection circuit furthermore comprises a fourth PMOS FET (MP4) that is connected so as to form a simultaneous switch together with the third PMOS FET (MP3), and whereby the drain of the fourth PMOS FET (MP4) is connected to the gate of the NMOS FET (MN1).

10. Voltage regulator according to Claim 1, whereby the input voltage shall be approximately 2.25 volts, and the target output voltage approximately 1.8 volts.

11. Voltage regulator according to Claim 1, whereby the level of the input voltage (Vdd) is raised from 0 volts when the voltage regulator is switched on.

12. Voltage regulator according to Claim 1, which is embodied in the form of an integrated circuit.

5